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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
09:756,867	01/10/2001	Hirotaka Nishizawa	XA-9415	6209	
75	90 04/15/2003				
MITCHELL W. SHAPIRO			EXAMINER		
MILES & STO	CKBRIDGE P. C. LE DRIVE		FUREMAN, JARED		
SUITE 500					
MCLEAN, VA	22102		ART UNIT	PAPER NUMBER	
			2876		

Please find below and/or attached an Office communication concerning this application or proceeding.

			$ L^{\Lambda_{i}}$
_	Application No.	Applicant(s)	
	09/756,867	NISHIZAWA ET AL.	
Office Action Summary	Examiner	Art Unit	
	Jared J. Fureman	2876	
The MAILING DATE of this communication a Period for Reply	appears on the cover sheet w	ith the correspondence address	S
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a - If NO period for reply is specified above, the maximum statutory peri - Failure to reply within the set or extended period for reply will, by sta - Any reply received by the Office later than three months after the ma earned patent term adjustment. See 37 CFR 1.704(b). Status	N. 1.136(a). In no event, however, may a lively within the statutory minimum of thire id will apply and will expire SIX (6) MON atute, cause the application to become Af	reply be timely filed ty (30) days will be considered timely. ITHS from the mailing date of this commun BANDONED (35 U.S.C.§ 133).	lication.
1) Responsive to communication(s) filed on \underline{C}	01 April 2003 .		
2a) This action is FINAL . 2b) ∑	This action is non-final.		
3) Since this application is in condition for allo closed in accordance with the practice und			erits is
Disposition of Claims	tion		
4) Claim(s) 1-28 is/are pending in the applicat		ration	
4a) Of the above claim(s) <u>8-11 and 14-28</u> is	are withdrawn from conside	ration.	
5) Claim(s) is/are allowed.			
6) Claim(s) <u>1-7,12 and 13</u> is/are rejected.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and Application Papers	d/or election requirement.		
9) ☑ The specification is objected to by the Exam	iner.		
10) ☐ The drawing(s) filed on 10 January 2001 is/a		ected to by the Examiner.	
Applicant may not request that any objection to		-	
11) The proposed drawing correction filed on	is: a)□ approved b)□ o	disapproved by the Examiner.	
If approved, corrected drawings are required in	reply to this Office action.		
12)☐ The oath or declaration is objected to by the	Examiner.		
Priority under 35 U.S.C. §§ 119 and 120			
13) Acknowledgment is made of a claim for fore	eign priority under 35 U.S.C.	§ 119(a)-(d) or (f).	
a)⊠ All b)□ Some * c)□ None of:			
1. Certified copies of the priority docum	ents have been received.		
2. Certified copies of the priority docum	ents have been received in A	Application No	
 3. Copies of the certified copies of the papplication from the International * See the attached detailed Office action for a 	Bureau (PCT Rule 17.2(a)).		je
14) Acknowledgment is made of a claim for dome	estic priority under 35 U.S.C.	§ 119(e) (to a provisional app	olication).
a) The translation of the foreign language 15) Acknowledgment is made of a claim for dom			
Attachment(s)	· -		
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s	5) Notice of	Summary (PTO-413) Paper No(s) Informal Patent Application (PTO-152	
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DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, having claims 1-7, 12, and 13 readable thereon, in Paper No. 6 is acknowledged. Claims 8-11 and 14-28 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claim Objections

2. Claims 1-4 are objected to because of the following informalities:

Re claims 1-3, line 1: "IC" should be replaced with --integrated circuit (IC)--, in order to clarify the claims.

Re claim 4:

Line 1, "the" (second occurrence) should be replaced with --a--, in order to avoid a lack of proper antecedent basis for "the connector terminal at one end".

Line 5, "adjoins the" should be replaced with --at one end adjoins a--, in order to clarify the claim.

Line 9, "the" first occurrence should be replaced with --a--, in order to avoid a lack of proper antecedent basis for "the connector terminal at the other end", and "the other" should be replaced with --a second--, in order to clarify the claim.

Line 12, "adjoins the" should be replaced with --at the second end adjoins a--, in order to clarify the claim.

Lines 13-14, "the other" should be replaced with --a second--, in order to clarify the claim.

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Appropriate correction is required.

Specification

3. The abstract of the disclosure is objected to because the abstract is greater than 150 words. Correction is required. See MPEP § 608.01(b).

- 4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
- 5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --INTEGRATED CIRCUIT CARD HAVING STAGGERED SEQUENCES OF CONNECTOR TERMINALS--.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 7. Claims 1-3 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamada (US 4,794,243).

Hamada teaches an integrated circuit (IC) card (A) comprising: a card substrate (printed circuit board 5) including a semiconductor integrated circuit chip (IC chip 2) mounted thereon; a plurality of connector terminals (3) formed thereon; the connector

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terminals being exposed from a casing (card body 1); wherein the connector terminals are laid out in plural sequences (L1, L2, L3, ...) in staggered form between the sequences adjacent to one another (L2 is staggered as compared to L1 and L3, see figure 1) forward and backward as viewed in an IC card inserting direction (the direction of the arrow in figure 3); wherein the connector terminals include an arrangement of two sequences (L1 and L2, for example) formed back and forth as viewed in an IC card inserting direction (the direction of the arrow in figure 3), and an arrangement of terminal-to-terminal areas (intervals α) of connector terminals laid out in a first sequence (L1) and an arrangement of terminal-to-terminal areas (intervals $\boldsymbol{\alpha})$ of connector terminals laid out in a second sequence (L2) are shifted from each other in a sequence direction (the direction perpendicular to the IC card inserting direction); wherein the connector terminals include an arrangement of two sequences (L1 and L2, for example) formed back and forth as viewed in an IC card inserting direction (the direction of the arrow in figure 3), and a sequence directional layout of connector terminals laid out in a first sequence (L1) and a sequence-directional layout of connector terminals laid out in a second sequence (L2) are shifted from each other in a sequence direction (the direction perpendicular to the IC card inserting direction); wherein a connector terminal sequence corresponding to a first sequence (L1) as viewed in an IC card inserting direction (the direction of the arrow in figure 3) has a connector terminal in which broad terminal-to-terminal distance (intervals α) is set to portions where the connector terminal faces a connector terminal sequence corresponding to a second sequence (L2) (see figures 1, 2A, 3, column 2 line 30 - column 3 line 6).

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Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada in view of Berg et al (US 6,142,802).

The teachings of Hamada have been discussed above.

Hamada fails to specifically teach wherein a connector terminal at one end extending in a sequence direction, of the connector terminals laid out in the second sequence extends to a position where the connector terminal at one end adjoins a connector terminal as viewed in a sequence direction, at one end extending in the sequence direction, of the connector terminals laid out in the first sequence, and a connector terminal at a second end extending in the sequence direction, of the connector terminals laid out in the second sequence extends to a position where the connector terminal at the second end adjoins a connector terminal as viewed in the sequence direction, at a second end extending in the sequence direction, of the connector terminals laid out in the first sequence.

Berg et al teaches an IC card (58) wherein a connector terminal (labeled A by the examiner in figure 8) at one end extending in a sequence direction, of connector terminals laid out in a second sequence (sequence labeled C by the examiner in figure 8) extends to a position where the connector terminal at one end adjoins a connector

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terminal as viewed in a sequence direction, at one end extending in a sequence direction, of connector terminals laid out in a first sequence (sequence labeled D by the examiner in figure 8), and a connector terminal (labeled B by the examiner in figure 8) at a second end extending in the sequence direction, of the connector terminals laid out in the second sequence extends to a position where the connector terminal at the second end adjoins a connector terminal as viewed in the sequence direction, at a second end extending in the sequence direction, of the connector terminals laid out in the first sequence (sequence labeled D by the examiner in figure 8) (see figure 8, column 5 lines 43-53, and column 6 lines 29-42).

In view of Berg et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the IC card as taught by Hamada, wherein a connector terminal at one end extending in a sequence direction, of the connector terminals laid out in the second sequence extends to a position where the connector terminal at one end adjoins a connector terminal as viewed in a sequence direction, at one end extending in the sequence direction, of the connector terminals laid out in the first sequence, and a connector terminal at a second end extending in the sequence direction, of the connector terminals laid out in the second sequence extends to a position where the connector terminal at the second end adjoins a connector terminal as viewed in the sequence direction, at a second end extending in the sequence direction, of the connector terminals laid out in the first sequence, in order to provide a connection sequencing function when electrical contact is made (see column 5 lines 51-53).

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10. Claims 5-7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada in view of Okayama et al (US 6,157,316) and Murohara (US 5,285,057).

The teachings of Hamada have been discussed above. Hamada also teaches a connector terminal sequence corresponding to a first sequence (L1) as viewed in an IC card inserting direction (the direction of the arrow in figure 3) has a connector terminal (one of terminals 3), and a connector terminal sequence corresponding to a second sequence (L2) has terminal-to-terminal areas (intervals α) at positions adjacent to the connector terminal (see figure 1).

Hamada fails to specifically teach wherein the connector terminals include one source supply terminal, two ground voltage supply terminals; wherein the connector terminals include data terminals corresponding to four bits and are provided as nine in total; wherein the connector terminals include data terminals corresponding to eight bits and are provided as thirteen in total; wherein a connector terminal sequence corresponding to a first sequence as viewed in an IC card inserting direction has a connector terminal for the supply of a source voltage, and a connector terminal sequence corresponding to a second sequence has terminal-to-terminal areas at positions adjacent to the connector terminal for the source voltage supply.

Okayama et al teaches an IC card (110) having connector terminals include one source supply terminal (pin 17), two ground voltage supply terminals (pins 1 and 34); wherein the connector terminals include data terminals corresponding to four bits (pins 2 and 30-32) and are provided as nine in total (the card has 68 pins, which includes 9 in total); wherein the connector terminals include data terminals corresponding to eight bits

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(pins 2-6 and 30-32) and are provided as thirteen in total (the card has 68 pins, which includes 13 in total); wherein a first connector terminal sequence (shown in figure 2A) has a connector (pin 17) for the supply of a source voltage (see figures 1, 2A, 2B, column 3 lines 19-30).

In view of Okayama et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the IC card as taught by Hamada, wherein the connector terminals include one source supply terminal, two ground voltage supply terminals; wherein the connector terminals include data terminals corresponding to four bits and are provided as nine in total; wherein the connector terminals include data terminals corresponding to eight bits and are provided as thirteen in total; wherein a connector terminal sequence corresponding to a first sequence as viewed in an IC card inserting direction has a connector terminal for the supply of a source voltage, and a connector terminal sequence corresponding to a second sequence has terminal-to-terminal areas at positions adjacent to the connector terminal for the source voltage supply, in order to make the IC card compatible with existing devices requiring certain terminals.

Hamada as modified by Okayama et al fails to specifically teach the connector terminals including one clock signal input terminal.

Murohara teaches an IC card having connector terminals (contact portion 4) including one clock signal input terminal (an operation clock supply terminal) (see figure 1 and column 2 lines 26-27, 37-39, and 48-56).

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In view of Murohara's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the IC card as taught by Hamada as modified by Okayama et al, the connector terminals including one clock signal input terminal, in order to provide synchronization between the IC card and a reader/writer device, thereby avoiding communication errors.

Conclusion

The prior art made of record and not relied upon is considered pertinent to 11. applicant's disclosure. Hamada (US 4,780,603), Takeda (US 4,532,419), Ohtsuki et al (US 4,695,914), Oguchi (US 6,527,590 B2), Lee et al (US 6,483,038 B2), Ono (JP 9-17511 A) and Asami (JP 4-152193 A) all teach IC cards having various connector terminal configurations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared J. Fureman whose telephone number is (703) 305-0424. The examiner can normally be reached on 7:00 am - 4:30 PM M-T, and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (703) 305-3503. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jared J. Fureman April 9, 2003

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